UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/816,955	04/05/2004	Satoshi Otsuka	042322	2296

38834 7590 05/25/2005

WESTERMAN, HATTORI, DANIELS & ADRIAN, LLP
1250 CONNECTICUT AVENUE, NW
SUITE 700
WASHINGTON, DC 20036

EXAMINER	
GEBREMARIAM, SAMUEL A	
ART UNIT	**PAPER NUMBER**
2811	

DATE MAILED: 05/25/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/816,955	OTSUKA, SATOSHI	
	Examiner	Art Unit	
	Samuel A. Gebremariam	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 March 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) *12-20* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *5/14/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of group I, claims 1-11 drawn to a semiconductor device is acknowledged.

Specification

2. The specification is replete with terms which are not clear, concise and exact. The specification should be revised carefully. Examples of some unclear, inexact or verbose terms used in the specification are: On page 4, line 12, the sentence "oxide film or an FSG film laid the later on the former" is not clear as to what it is stating. Page 9, first paragraph "interconnection layers 344a, 344b buried in, an inter-layer insulation film 346 of a silicon nitride film and a silicon oxide film laid on the latter of the formed is formed. The above sentence appears to grammatically incorrect. These types of sentences appear through out the specification. And also on page 7, line 24; the specification refers to layer 336 as the interconnection layer. However layer 336 is labeled as an inter layer insulation layer in fig. 17. Appropriate correction is required.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> **The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.**

Claim 10 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The limitation of "the diffusion preventing film of one second inter-layer insulation film being formed directly on the second low dielectric constant film

of another second inter-layer insulation film underlying said one second inter-layer insulation film" is not clear as what it is referring to. It is not clear what the term "another second interlayer insulation film is referring to. There appears to be one second interlayer insulation layer, but it not clear what the other second interlayer insulation film is referring to.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> **(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.**

5. Claims 1, 3, 5 and 8-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Miyamoto et al. US patent No. 6,670,714 in view of Chiang et al. US patent No. 5,739,579.

Regarding claim 1, Miyamoto teaches a semiconductor device comprising: a first inter-layer insulation film (18) formed over a substrate (11) and including a first low dielectric constant film (18); a first interconnection layer (19) buried in a first inter-layer interconnection trench (col. 4, lines 58-63) formed in the first insulation film (18), whose minimum interconnection pitch is first pitch (refer to fig. 4); a second inter-layer insulation film (23 and the layer above it) formed over the first inter-layer insulation film (18) and including a second low dielectric constant film (layer 23 and the layer above it have a dielectric constant); a second interconnection layer (the interconnection layer in the middle part of fig. 4) buried in a second interconnection trench formed (col. 4, lines

58-63) in second inter-layer insulation film, whose minimum interconnection pitch a second pitch larger than the first pitch (refer to fig. 4); a film (the thin layer that is formed over the middle interconnection that is formed directly both on the second dielectric and the interconnection in the middle) and a film formed directly on second low dielectric constant film and the second interconnection layer (refer to fig. 4).

Miyamoto does not explicitly teach forming a hydrophilic insulation film formed on first low dielectric constant film or forming a diffusion preventing film.

Chiang teaches (fig. 25) the use of silicon nitride layer (323) and silicon oxide layer (322) in a structure of forming an interconnection structure.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the silicon nitride layer taught by Chiang in the structure of Miyamoto in order to provide a better diffusion barrier property (col. 2, lines 49-62). Furthermore the combined structure of Miyamoto and Chiang inherently provides a low dielectric constant film (silicon oxide) and a hydrophilic insulation film (silicon nitride) formed on the low dielectric constant film. The combined structure of Miyamoto and Chiang also teaches diffusion preventing film (silicon nitride) formed directly on second low dielectric constant film (23) and the second interconnection layer.

Regarding claim 3, Miyamoto teaches substantially the entire claimed structure of claim 1 above including a diffusion preventing film (15) formed directly on the hydrophilic insulation film (11) and the first interconnection layer (14) (refer to fig. 1 of Kajita).

Regarding claim 5, Miyamoto teaches substantially the entire claimed structure of claim 1 above except explicitly stating that the second pitch is 1.5 or more times the first pitch.

Parameters such as pitch and width in the art of semiconductor manufacturing process are subject to routine experimentation and optimization to achieve the desired device characteristics during fabrication.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to adjust the first and second pitch as claimed in order to form an interconnection that is better protected from diffusion of water.

Regarding claim 8, Miyamoto teaches substantially the entire claimed structure of claim 1 above including the interconnection layer (fig. 4 of Miyamoto) is buried in a via hole formed the inter-layer insulation film and in the interconnection trench formed in a region of the inter-layer insulation film, which includes the via hole (refer to fig. 4 of Miyamoto).

Regarding claim 9, Miyamoto teaches substantially the entire claimed structure of claim 1 above including the main material of the interconnection layer is Cu (col. 5, lines 10-20, Miyamoto).

Regarding claim 10, as best the examiner is able to ascertain the claimed invention, Miyamoto teaches (fig. 4) a semiconductor device comprising: a first multilayer interconnection layer (bottom interconnection, fig. 4) formed over substrate (11) and including plurality interconnection layers whose minimum interconnection pitch is first pitch (fig. 4); and a second multilayer interconnection layer (middle

interconnection) formed over the first multilayer interconnection layer and including minimum interconnection layers whose interconnection pitch is a second pitch larger than the first pitch (bottom interconnection is has smaller pitch than the middle, refer to fig. 4), at least one of the plurality of interconnection layers (bottom) forming the first multilayer interconnection layer being buried an opening formed in first inter-layer insulation film (18) including a first low dielectric constant film (layer 18 has a dielectric constant) and, the respective plurality of interconnection layers forming the second multilayer interconnection layer being buried in an opening formed in a second inter-layer insulation film (layer 23 and the layer above it) including a film (the layer formed above layer 23 and the layer above it) and a second low dielectric constant film formed on the film (there are a plurality of layer 23 formed above the second interlayer insulating layer).

Miyamoto does not explicitly teach a hydrophilic insulation film formed on the first low dielectric constant film or a diffusion preventing and the diffusion preventing film one second inter-layer insulation film being formed directly on the second low dielectric constant film of another second inter-layer insulation film underlying said one second inter-layer insulation film.

Chiang teaches (fig. 25) the use of silicon nitride layer (323) and silicon oxide layer (322) in a structure of forming an interconnection structure.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the silicon nitride layer taught by Chiang in the structure of Miyamoto in order to provide a better diffusion barrier property (col. 2, lines

49-62). Furthermore the combined structure of Miyamoto and Chiang inherently provides a low dielectric constant film (silicon oxide) and a hydrophilic insulation film (silicon nitride) formed on the low dielectric constant film. The combined structure of Miyamoto and Chiang also teaches diffusion preventing film (silicon nitride) formed directly on second low dielectric constant film (23) and the second interconnection layer.

Claims 2, 4, 6 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Miyamoto, Chiang and in view of Kajita, US patent No. 6,573,604.

Regarding claim 2, Miyamoto teaches substantially the entire claimed structure of claim 1 above including a third inter-layer insulation film (the interlayer insulating layer formed on the top portion of the interconnection structure) formed over the second inter-layer insulation film (the inter layer in the middle); and third interconnection layer (the interconnection layer on the top portion of the interconnect structure) buried in a third trench formed in the third inter-layer insulation film (refer to fig. 4), whose minimum interconnection pitch is a third pitch larger than the first pitch and second pitch (refer to fig. 4).

Miyamoto does not explicitly teach that the third interlayer isolation film includes an insulation film having dielectric constant higher than the first low dielectric constant film and the second low dielectric constant film.

It is conventional and also taught by Kajita to use of interlayer insulation layers with different dielectric constants on top of each other in the structure of forming an interconnection (fig. 1).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to select the third interlayer dielectric layer from one of the interlayer dielectric layers taught by Kajita in the structure Miyamoto in order to prevent water from diffusing into the integrated circuit structure. The combined structure of Miyamoto, Chiang and Kajita inherently teaches a third interlayer isolation film having dielectric constant higher than the first low dielectric constant film and the second low dielectric constant film.

Regarding claim 4, Miyamoto teaches substantially the entire claimed structure of claim 2 above including a diffusion preventing film (15) formed directly on the hydrophilic insulation film (11) and the first interconnection layer (14) (refer to fig. 1 of Kajita).

Regarding claim 6, Miyamoto teaches substantially the entire claimed structure of claim 2 above except explicitly stating that the second pitch is 1.5 or more times the first pitch.

Parameters such as pitch and width in the art of semiconductor manufacturing process are subject to routine experimentation and optimization to achieve the desired device characteristics during fabrication.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to adjust the first and second pitch as claimed in order to form an interconnection that is better protected from diffusion of water.

Regarding claim 11, Miyamoto teaches substantially the entire claimed structure of claim 10 above including a third multilayer interconnection layer (the upper

interconnection layer of fig. 4) formed over the second multilayer interconnection layer (layer 23 and the layer above it, fig. 4) and including a plurality of interconnection layers whose minimum interconnection pitch a third pitch larger than the first pitch and the second pitch (the upper interconnection layers have larger pitch than the bottom and the middle interconnection layer), the plurality of interconnection layers forming the third multilayer interconnection layer being buried in an opening formed in a third inter-layer insulation film (refer to fig. 4).

Miyamoto does not explicitly teach the third interlayer insulation film having a higher dielectric constant than the first low dielectric constant film and the second low dielectric constant film.

It is conventional and also taught by Kajita to use of interlayer insulation layers with different dielectric constants on top of each other in the structure of forming an interconnection (fig. 1).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to select the third interlayer dielectric layer from one of the interlayer dielectric layers taught by Kajita in the structure Miyamoto in order to prevent water from diffusing into the integrated circuit structure. The combined structure of Miyamoto, Chiang and Kajita inherently teaches a third interlayer isolation film having dielectric constant higher than the first low dielectric constant film and the second low dielectric constant film.

6. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Miyamoto, Chiang in view of Ong, US PUB. No. 2004/0104481 A1.

Miyamoto teaches substantially the entire claimed structure of claim 1 above except explicitly stating that the low dielectric constant film is an SiOC film, a SiLK film, a BCB film, a FLARE film or a porous silicon oxide film.

Ong teaches the use of low dielectric materials such as SiOC in the process of forming interconnection [0005].

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the low dielectric constant material taught by Ong in the structure of Miyamoto in order to reduce RC delay.

Conclusion

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Samuel A Gebremariam whose telephone number is (571) 272-1653. The examiner can normally be reached on 8:00am-4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on (571) 272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

SAG
May 13, 2005

EDDIE LEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800